REMARKS/ARGUMENT

Applicants appreciate the Examiner's determination that Claim 39 would be allowable if rewritten or amended to overcome the objection to the claim. Claim 39 has been amended to comply with the Examiner's recommendation. Accordingly, the objection to Claim 39 is overcome and Claim 39 stands allowable.

Claims 11 and 27 have been amended better to define the claimed invention and overcome the 35 U.S.C. 112, second paragraph, rejection. Accordingly, the 35 U.S.C. 112, second paragraph, rejection of Claims 11-13 and 27-28 is overcome.

1) Claims 1-49 stand rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-57 of co-pending Application No. 10/616,207. Applicants respectfully traverse this rejection as set forth below.

In rejecting Claims 1-49, the Examiner has not compared Claims 1-49 of the present application with Claims 1-57 of copending Application No. 10/616,207. Applicants respectfully submit that the Examiner has not established a prima facie case of obviousness-type double patenting for Claims 1-49. In order to establish a prima facie case of obviousness-type double patenting, **the Examiner must establish that the claims of the present application are obvious over the CLAIMS of the cited patent** (in the present case, a co-pending application). The Examiner has made a general allegation but no claim to claim comparison. Applicants direct the Examiner's attention to MPEP § 804(B)(1):

> In determining whether a nonstatutory basis exists for a double patenting rejection, the first question to be asked is – **does <u>any claim in the application</u> define an invention that is merely an obvious variation of an <u>invention claimed in the patent</u>**? If the answer is yes, then an "obvious-type" nonstatutory double patent rejection may be appropriate.

(A) **Determine the scope and content of a patent claim** and the prior art **relative to a claim in the application** at issue;

(B) **Determine the differences between the scope and content of the patent claim and the prior art as determined in (A) and the claim in the application at issue;**

(C) Determine the level of ordinary skill in the pertinent art; and

(D) Evaluate any objective indicia of nonobviousness.

The conclusion of obvious-type double patenting is made in light of these factual determinations.

Any obvious-type double patent rejection should make clear:

(A) The **differences between the inventions defined by the conflicting claims - a claim in the patent compared to a claim in the application**; and

(B) The reasons why a person of ordinary skill in the art would conclude that the invention **defined in the claim in issue is an obvious variation of the invention defined in a claim in the patent.**

When considering whether the invention defined in a claim of an application is an obvious variation of the invention defined in the claim of a patent, **the disclosure of the patent may not be used as prior art.** This does not mean that one is precluded from all use of the patent disclosure.

In lieu of the above, it is clear that the Examiner has not set forth a prima facie case that Claims 1-49 of the present application are obvious over claims 1-57 of co-pending Application No. 10/616,207.

2) Claims 1, 7, 12, 13 and 15 stand rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (USP 6,437,623). Applicants respectfully traverse this rejection, as set forth below.

Applicants are confused by the Examiner's above rejection. The Examiner rejects Claims 1, 7, 12, 13 and 15 above, yet in the Examiner's discussion on page 3, line 21 – page 4, line 10, the Examiner further discusses Claims 11 and 14. For the purposes of this response, Applicants will assume the Examiner meant to reject Claims 1, 7 and 11-15.

In order that the rejection of Claims 1, 7 and 11-15 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites a data latch apparatus , comprising: "a first latch for latching a data signal", "a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative", "**a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**".

Independent Claim 11, as amended, requires and positively recites a data processing apparatus, comprising: "data processing logic for performing data processing operations", "a plurality of registers coupled to said data processing logic for storing data associated with said data processing operations, each said register including a data latch structure", "each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and **a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**".

Independent Claim 14 requires and positively recites, a wireless communication apparatus, comprising: "an antenna structure for permitting communication via an air interface", "a digital data processor for performing digital data processing operations", "a wireless communication interface coupled between said antenna structure and said digital data processor for interfacing between said antenna structure and said digital data processor", "said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and **a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**".

In contrast, the Hsu reference discloses an apparatus having a master latch (21) connected via mux2 (26) to a slave latch (22) and a data retention latch (24). A feedback loop (FL) connects data retention latch (24) to the master latch (21). There is no teaching in Hsu whatsoever that Mux1 (25) is a restore device or that it affects restoration of the data from data retention latch (24) to master latch (21). Moreover, even if, arguendo, Mux1 (25) were to be a restore device, there is no teaching or suggestion in Hsu that Mux1 (25) is powered by a power supply other than the power supply for data retention latch (24). As such, Hsu fails to teach or suggest, "**a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**", as required by Claim 1, or "each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and **a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than**

said first power supply", as required by Claim 11, or "said digital data processor including a plurality of data latch structures, each said data latch structure including a first latch for latching a data signal, a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative, and **a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**", as required by Claim 14. As a result, the 35 U.S.C. 102(e) rejection of Claims 1, 11 and 14 as being anticipated by Hsu is overcome.

Claims 7, 12, 13 and 15 stand allowable as depending (directly or indirectly) from allowable claims and including further limitations not taught or suggested by the reference of record.

Claim 7 further defines the apparatus of Claim 1, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom. Claim 7 stands allowable for the same reasons Claim 1 stands allowable. Moreover, Hsu fails to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 1.

Claim 12 further defines the apparatus of Claim 11, provided as one of a microprocessor, a microcontroller and a digital signal processor. Claim 12 stands allowable for the same reasons Claim 11 stands allowable. Moreover, Hsu fails to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 11.

Claim 13 further defines the apparatus of Claim 11, including a logic signal path connected to said restore devices for distributing said first power supply thereto. Claim 13 stands allowable for the same reasons Claim 11 stands allowable. Moreover, Hsu fails

to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 11.

Claim 15 further defines the apparatus of Claim 14, provided as one of a mobile telephone, a laptop computer and a personal digital assistant. Claim 15 stands allowable for the same reasons Claim 14 stand allowable. Moreover, Hsu fails to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 14.

3) Claims 1 and 6-8 stand rejected under 35 U.S.C. 102(e) as being anticipated by Hsu et al. (USP 6,437,623). Applicants respectfully traverse this rejection, as set forth below.

In order that the rejection of Claims 1 and 6-8 be sustainable, it is fundamental that "each and every element as set forth in the claim be found, either expressly or inherently described, in a single prior art reference." Verdegall Bros. v. Union Oil Co. of California, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). See also, Richardson v. Suzuki Motor Co., 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), where the court states, "The identical invention must be shown in as complete detail as is contained in the ... claim".

Furthermore, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Independent Claim 1 requires and positively recites a data latch apparatus , comprising: "a first latch for latching a data signal", "a second latch coupled to said first latch for retaining said data signal while said first latch is inoperative", "**a restore device**

connected between said first and second latches and driven by a first power supply for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**".

In contrast, the Zyuban reference discloses an apparatus having a master latch (50) connected to a scan/retention latch (60). A feedback path (22) connects an output of scan/retention latch (60) to the master latch (50). There is no teaching in Zyuban whatsoever that multiplex 21 is a restore device or that it affects restoration of the data from scan/retention latch (60) to master latch (50). Indeed, Zyuban specifically teaches, "the path for restoring data from the retention latch to the main latch is implemented as line 22 passing through multiplexer 21" (page 3, paragraph 27, lines 11-13). Moreover, Zyuban further teaches, "the combination of line 22 and the transistors that pass the state of latch 60 to latch 50 will be referred to as "data restore means"" (page 3, paragraph 27, lines 14-16). Accordingly, multiplexer 21 cannot be equated to a "restore device". Moreover, even if, arguendo, latch 50 were to be a restore device, there is no teaching or suggestion in Zyuban that latch 50 is powered by a power supply other than the power supply for scan/retention latch (60). As such, Zyuban fails to teach or suggest, "**a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**", as required by Claim 1. As a result, the 35 U.S.C. 102(e) rejection of Claim 1 as being anticipated by Zyuban is overcome.

Claims 6-8 stand allowable as depending (directly or indirectly) from allowable Claim 1 and including further limitations not taught or suggested by the reference of record.

Claim 6 further defines the apparatus of Claim 1, wherein said second latch includes a node for providing said data signal to said restore device, said restore device

including a transistor having a gate connected to said node. Claim 6 stands allowable for the same reasons Claim 1 stands allowable. Moreover, Zyuban fails to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 1.

Claim 7 further defines the apparatus of Claim 1, wherein said second latch is for retaining said data signal while said first latch is inoperative due to removal of power therefrom. Claim 7 stands allowable for the same reasons Claim 1 stands allowable. Moreover, Zyuban fails to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 1.

Claim 8 further defines the apparatus of Claim 1, wherein said second latch includes first and second nodes for providing said data signal to said restore device, said restore device including first and second transistors having respective gates connected to said first and second nodes, respectively. Claim 8 stands allowable for the same reasons Claim 1 stands allowable. Moreover, Zyuban fails to teach or suggestion this additional requirement in combination with previously discussed requirements of Claim 1.

4) Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Hsu et al. (USP 6,437,623) in view of Schober (USP 6,333,656). Applicants respectfully traverse this rejection, as set forth below.

In proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing In re Piasecki, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge**

generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references", In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing In re Fine, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing In re Lalu, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Claim 2 further defines the apparatus of Claim 1, wherein said second latch includes a first node for providing said data signal to said restore device, said restore device including first and second transistors having respective gates connected to said first node.

As argued above, the Hsu reference discloses an apparatus having a master latch (21) connected via mux2 (26) to a slave latch (22) and a data retention latch (24). A feedback loop (FL) connects data retention latch (24) to the master latch (21). There is no teaching in Hsu whatsoever that Mux1 (25) is a restore device or that it affects restoration of the data from data retention latch (24) to master latch (21). Moreover, even if, arguendo, Mux1 (25) were to be a restore device, there is no teaching or suggestion in Hsu that Mux1 (25) is powered by a power supply other than the power supply for data retention latch (24). As such, Hsu fails to teach or suggest, "**a restore device connected between said first and second latches and driven by a first power supply** for transferring said data signal from said second latch to said first latch" and "said second latch **powered by a second power supply other than said first power supply**", as required by Claim 1, from which Claim 2 depends.

Even if, arguendo, the Schober's figure 4 shows a Flip Flop circuit having output buffer (M41-M44) coupled to an output of a latch (slave latch) for the purpose of improving the output strength, as suggested by the Examiner, Schober fails to overcome the previously identified deficiencies of the Hsu reference. As such, Claim 2 is allowable for the same reasons Claim 1 is allowable.

Applicants appreciate the Examiner's determination that: a) Claims 3-5 and 9-10 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims, and rewritten or amended to overcome the Double Patenting rejection; b) Claims 16-26, 29-38 and 40-49 would be allowable if rewritten or amended to overcome the Double Patenting rejection; and c) Claims 27-28 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, rejection and rewritten or amended to overcome the Double Patenting rejection above. Applicants have amended Claims 27-28 to overcome the 35 U.S.C. 112, second paragraph, rejection. For the reasons provided in this response, however, Applicants respectfully submit that Claims 1-49 are allowable in their present form.

Objected to Claim 39 has been amended to be allowable. Claims 11 and 27 have been amended to overcome the 35 U.S.C. 112, second paragraph, rejection. Accordingly, Claims 1-49 stand allowable. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

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